Invited Speaker for ICCSEEA2023

Dr. Jing Zuo

Dr. Zuo Jing is an associate professor and the director of the Quality Assessment Office at Nanning University, China. She is an FDW International Certification Teaching Skills Instructor, a Level One Certified TRIZ Specialist, a certified entrepreneurship mentor from Stanford, a national second-level entrepreneurship consultant, and one of the first excellent innovation and entrepreneurship mentors in the autonomous region. She is also a teaching skills exam testing expert for higher education teachers' qualifications in Guangxi.

Her research interests include quality assessment and the development of university teachers. She has published over 30 papers and has led and participated in multiple research projects, including pre-job training system reforms for university teachers, the development of teaching abilities and the improvement of classroom teaching quality for university teachers, and the research on academic evaluation models for university teachers.

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Title: Research on the Influencing Factors of Students' General Competency Improvement in Application-Oriented Universities

Speaker: Jing Zuo

Abstract: Students' competency cultivation is a very important measure of the effectiveness of talent development. In order to explore the influencing factor of student's general competency in application-oriented Universities, this study take 9652 students from different majors in one application-oriented University as sample,

regression analysis has been applied with a dependent variable (general competency improvement) and six independent variables (student's learning behavior: in-class, after-class, interact with classmates; teacher's teaching behavior; evaluation of teaching content; professional identity) to sort out the influencing factors. The results show that teacher's teaching behavior, evaluation of teaching content, student's learning behavior (in-class, after-class, and interact with student), and professional identity is significantly positively related to the improvement of students' general competency; especially, the teacher's teaching behavior, and evaluation of teaching content, these are the key factors of student's general competency improvement.

Invited Speaker for ICCSEEA2023

Prof. Artem Volokyta

Associate professor Artem Volokyta, Department of Computer Engineering, National Technical University of Ukraine, “Igor Sikorsky Kyiv Polytechnic Institute”, Ukraine.

(ORCID ID https://orcid.org/0000-0001-9069-5544)

Major interests: High-performance computer systems and networks: theory, methods and means of hardware and software implementation; design of fault-tolerant distributed computing systems; network topological organization.

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Title: Methods of Topological Organization Synthesis based on Tree and Dragonfly Combinations

Speaker: Artem Volokyta

Abstract: The paper is devoted to consideration of several ways to synthesis new topological organizations based on different types of trees and Dragonfly sequences. Various combinations of combining standard topologies with Dragonfly topology, which allows obtaining new fault-tolerant topologies with specified properties, are proposed. The characteristics of the synthesized topologies are investigated, their advantages and disadvantages are shown. The presented variants of topologies can be the basis for the design of fault-tolerant survivable scalable systems. Developing a system using this approach will increase fault tolerance and topological characteristics that directly influence the overall performance of distributed applications.

Invited Speaker for ICCSEEA2023

Prof. Maksim Iavich

In 2001 – 2005 studied in Ivane Javakhishvili State University of Tbilisi, Georgia at the faculty of Computer sciences and of qualification of expert in informatics and got the bachelor degree. In 2006 – 2009 studied in the same University at the same faculty, got the master's degree. In 2010 – 2014 studied in the Georgian Technical University at the faculty of informatics and Control Systems, got the PH.D. degree. The topic was: Mathematical model of educational social networks and their use in teaching process. In 2009 passed the Diplomatic Seminar of young Jewish leaders, organized by Ministry of Foreign Affairs in Jerusalem and got the certificate. In 2014 made cryptography course provided by Stanford University and got certificate. In 2014 – 2015 made Cyber Security specialization (usable security, software security, cryptography, hardware security and capstone project) provided by University of Maryland and got specialization. In 2016 -2018 has graduated from many programming and cyber security courses provided by different leading Universities and got the corresponding certificates.

Work experience: In 2002 worked in USA in Eisner Camp as a counselor. In 2003 began to work in Jewish school Tiferet-Zvi as the computer teacher. In 2009-2014 worked in Maalot Zeidner Institute as computer science lecturer. In 2011-2013 worked in Georgian Technical University as a major teacher. In 2014 worked in Georgian Technical University as associate professor. In 2012-2014 worked in Or Avner school as computer teacher. In 2009-2015 was a director of computer center LTD "Maxitop". In 2014- 2017 was a head of computer science bachelor program in Georgian Bank University. In 2015-2017 was involved in post-quantum cryptography scientific project as a young researcher. Now he is involved as researcher in "digital signature schemes

in post-quantum war" scientific project. He uses to be the invited speaker at international cyber security conferences; Maksim is the IT consultant in international organizations. Since 2015 works in Georgian Technical University as invited professor. In 2014- 2015 worked in Caucasus University as associate professor. Since 2015 is professor in this university. Since 2018 is affiliate professor and the head of cyber security direction in Caucasus University. Maksim is the author of many scientific papers. The topics of the papers are: cyber security, cryptography, post-quantum cryptography, quantum cryptography, mathematical models and simulations.

Winner of the best young scientist award by Shota Rustaveli national foundation in 2018. Got the best paper award on international scientific conferences IVUS 2018 and IVUS 2019 in Lithuania.

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Title: Machine learning based function for 5G working with CPU threads

Speaker: Maksim Iavich

Abstract: A huge amount of information is transmitted over wireless networks. Moreover, the volume of transmitted information is constantly increasing, one of the many factors in this is that new mobile devices are continuously communicate with each other through the network, and the number of multimedia applications, streaming, video conferencing, social networks and other things are growing behind them. To meet current and expected needs, Transition to 5G networks is taking place at great pace. As of 2021 and 2022, approximately one million minutes of video per second was transmitted over the Internet worldwide, and as data grows rapidly, the 4G system needs to be replaced with a more powerful 5G system with increased bandwidth and improved quality of service to ensure a secure and stable connection. 5G have the security problems. During our research, we were able to identify various 5G security vulnerabilities and then study them in detail. On the basis of which we have implemented a new machine learning based cybersecurity model with its Firewall and IDS/IPS, which we describe in this article. We have analyzed the use of different machine learning algorithms for our task. Finally, decision tree algorithm was chosen. We have implemented this algorithm using CPU threads to increase the efficiency. The main significance of the offered security function is that it is very efficient and works

very quickly; therefore, it can be considered for real time usage. The offered security function is trained with attack patterns created in a simulation lab. We have tested this mechanism in the simulated 5G network. The experiment was carried out in our laboratory, where we used 10 Raspberry Pi modems to simulate attacks on the server. A similar approach will be useful for future versions of 5G.

Invited Speaker for ICCSEEA2023

Oleksii Dovhaniuk

Oleksii Dovhaniuk is a researcher in the School of Computer Science, University College Cork, Ireland. He completed his education as a Computer Engineer at Yuriy Fedkovich Chernivtsi National University, where he also received a master's degree in engineering with a focus on IoT Technologies and Cyber-physical Systems. During his academic pursuits, Oleksii spent a semester studying in Germany as an exchange student and also studied in Austria for his master's degree. Oleksii engaged in various scientific endeavors focused on advanced computing since his bachelor's study, such as attending the ECODAM and IEEE International Conference on Electronics and Information Technologies. During his research, he designed a genetic algorithm for producing reversible circuits, which are more energy-efficient and less prone to faults than traditional circuitry.

Currently, Oleksii is collaborating with Professor Sabin Tabirca to create a medical resource scheduling application specifically for operating theatres in surgical procedures. They are merging Oleksii's expertise in evolutionary computing for optimal solutions and deep learning prediction models to develop an automated and efficient scheduler suitable for implementation in hospitals.

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Title: The Extended Fredkin Gates with Reconfiguration in NCT Basis

Speaker: Oleksii Dovhaniuk

Abstract: The Fredkin gate is a universal reversible logic gate widely used in designing low-power and quantum devices of various complexities. Recently, the gate's extension was proposed based on its elementary components. It provided variety in

functionality and, at the same time, preserved the main features of the gate. This paper offers additional variations of the Fredkin gate, referring to the recent findings. The versatility of logic circuits is particularly beneficial in programmable logic. Therefore, a reconfiguration for the proposed gates has been designed. The device includes 24 newly obtained gates and 8 known extensions. The reconfigurable circuit has a significant advantage in flexibility over the classic gate of 32 extended 3-bit Fredkin gates with a relatively small increase in hardware complexity and delay time. The implementation of the circuit has been tested and verified in Active-HDL, confirming the design's correctness. Reconfigurable devices synthesized in the work make it possible to create programmable fault-tolerant reversible logic circuits effectively.